REMARKS

Claim Amendments

Applicant has amended independent claims 1, 7, 12 and 15 to include the limitations of dependent claims 4, 9, 14 and 19. No new material has been added.

Formal Rejection

While not agreeing with the Examiner's formal objections, the claims have been amended to expedite prosecution. Accordingly, each claim is now deemed to be in condition for allowance.

Claim Rejection

Claims 1-24 are pending. Of those, claims 1-3, 5-8, 10-13, 15-18 and 20 stand rejected as allegedly anticipated by USPN 5,081,373 to Suzuki ("Suzuki"). Applicant asserts that the rejection is improper and should be withdrawn.

Examiner has issued his rejection based on 35 U.S.C. § 102(b). However, for a Section 102 rejection to be proper, each and every element of the claim must be present in the cited art. Independent claims 1, 7, 12, 15, and 21-24 all recite in pertinent parts, "wherein at least one of the first or the second signal passing module **is a NAND gate**." Figure 1 of Suzuki neither discloses nor implies a NAND gate. Additionally, Suzuki neither discusses nor suggests a NAND gate as a signal passing module at any point in the disclosure.

Examiner states that the combinations of AND gates 131 and 132 of Suzuki with inverters 141 and 142 of Suzuki constitute NAND gates when the RST signal is not used. This

conclusion is inaccurate for several reasons. First, elements 141 and 142 of Suzuki are NOR gates, with RST signal inputs, not inverters as stated. Whether or not the RST signal is used, 141 and 142 will continue to act as NOR gates. Therefore, Suzuki does not contain the same elements as claims 1, 7, 12, 15 or 21-24 and cannot properly anticipate them.

Second, combining an AND gate and a NOR gate neither produces the same output as, nor includes the same components as a NAND gate. In other words, a combination of an AND gate and a NOR gate is not the functional equivalent of a NAND gate. A NAND gate is a single component and therefore requires fewer components than an AND gate combined with a NOR gate. Therefore, using a single NAND gate provides the advantages of lower costs and higher efficiency over combining an AND gate and a NOR gate.

Third, as amended herein, the NAND gate of independent claims 1, 7, 12, 15 and 21-24 include a flag signal input. This flag signal is functionally different from the preset PST and reset RST signal inputs of Suzuki. "[T]he flag identifies the power status of the circuit to prevent leakage problems when the flip-flop is not in operation," [Paragraph 0011]. By comparison, the PST signal is used to initialize the signal passing portion (Col 5, Line 32-33) and the reset signal is used to clear the hold data of the signal passing portion (Col 5, Line 32-35). Therefore, because Suzuki neither discloses nor implies a flag signal, Suzuki can not anticipate Applicant's claims.

Claims 5, 6, 10-14, 20 and 23 stand rejected as allegedly obvious over Suzuki in view of Weste *et al.* (Principles of CMOS VLSI Design: A Systems Perspective, 1993, Addison-Wesley Publ'g Co., 2nd ed, page 91). However, as stated above, Suzuki does not disclose or imply all the elements of Applicant's claims and therefore can not anticipate them. Further, Suzuki *teaches away* from using a single NAND gate and a flag signal and requires instead a PST and

RST signal. Additionally, West *et al.* discloses only a method of construction of tristate inverters. Therefore, claims 5, 6, 10-14 and 20-23 can not be obvious over Suzuki in view of West *et al.*

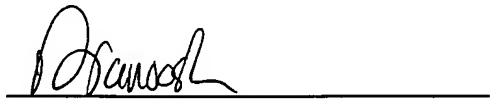
Because dependent claims 2-4, 8-9, and 16-19 depend from otherwise allowable claims, Applicant asserts that they are also allowable.

In view of the amendments and remarks provided herein, reconsideration and withdrawal of the anticipation rejection is respectfully requested.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance. While an extension of time is not deemed necessary, the Office is requested and hereby authorized to charge the appropriate extension-of-time fees against Account No. 04-1679 to Duane Morris LLP. The Examiner is invited to contact the undersigned to discuss any issue relating to this application.

Respectfully Submitted,



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Dated: November 28, 2005